539,224

(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
8 July 2004 (08.07.2004)

PCT

(10) International Publication Number
WO 2004/057659 A1

(51) International Patent Classification[7]: H01L 21/28, 21/336, 21/285

(21) International Application Number: PCT/IB2003/006009

(22) International Filing Date: 15 December 2003 (15.12.2003)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
02080508.1 20 December 2002 (20.12.2002) EP

(71) Applicant *(for all designated States except US)*: **KONINKLIJKE PHILIPS ELECTRONICS N.V.** [NL/NL]; Groenewoudseweg 1, NL-5621 BA Eindhoven (NL).

(71) Applicant *(for DE, FR, GB, JP only)*: **INTERUNIVERSITAIR MICROELEKTRONICA CENTRUM VZW** [BE/BE]; Kapeldreef 75, B-3001 Leuven (BE).

(72) Inventors; and

(75) Inventors/Applicants *(for US only)*: **VENEZIA, Vincent, C.** [US/BE]; c/o Prof . Holstlaan 6, NL-5656 AA Eindhoven (NL). **DACHS, Charles, J., J.** [FR/BE]; c/o Prof . Holstlaan 6, NL-5656 AA Eindhoven (NL). **HOOKER, Jacob, C.** [US/BE]; c/o Prof . Holstlaan 6, NL-5656 AA Eindhoven (NL). **VAN DAL, Marcus, J., H.** [NL/BE]; c/o Prof . Holstlaan 6, NL-5656 AA Eindhoven (NL).

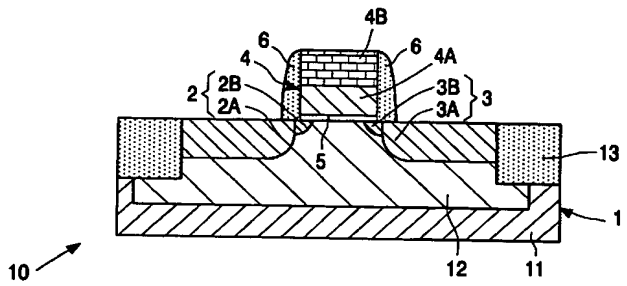
(74) Agent: **DULJVESTIJN, Adrianus, J.**; Philips Intellectual Property & Standards, Prof. Holstlaan 6, NL-5656 AA Eindhoven (NL).

(81) Designated States *(national)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM, ZW.

(84) Designated States *(regional)*: ARIPO patent (BW, GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, BG, CH, CY, CZ, DE, DK, EE,

[Continued on next page]

(54) Title: METHOD OF MANUFACTURING A SEMICONDUCTOR DEVICE AND SEMICONDUCTOR DEVICE OBTAINED WITH SUCH A METHOD



(57) Abstract: The invention relates to a method of manufacturing a semiconductor device (10) with a field effect transistor, in which method a semiconductor body (1) of a semiconductor material is provided, at a surface thereof, with a source region (2) and a drain region (3) and with a gate region (4) between the source region (2) and the drain region (3), which gate region comprises a semiconductor region (4A) of a further semiconductor material that is separated from the surface of the semiconductor body (1) by a gate dielectric (5), and with spacers (6) adjacent to the gate region (4), for forming the source and drain regions (2,3), in which method the source region (2) and the drain region (3) are provided with a metal layer (7) which is used to form a compound (8) of the metal and the semiconductor material, and the gate region (4) is provided with a metal layer (7) which is used to form a compound (8) of the metal and the further semiconductor material. The known method in which different metal layers are used to silicidate source and drain regions and gate regions (2,3,4) has several drawbacks. A method according to the invention is characterized in that before the spacers (6) are formed, a sacrificial region (4B) of a material that may be selectively etched with respect to the semiconductor region (4A) is deposited on top of the semiconductor region (4A), and after the spacers (6) have been formed, the sacrificial layer (4B) is removed by etching, and after removal of the sacrificial layer (4B), a single metal layer (7) is deposited contacting the source, drain and gate regions (2,3,4). This method is on the one hand very simple as it requires only a single metal layer and few, straight-forward steps and it is compatible with existing (silicon) technology, and on the other hand it results in a (MOS)FET which does not suffer from a depletion layer effect in the fully silicided gate (4).

WO 2004/057659 A1

ES, FI, FR, GB, GR, HU, IE, IT, LU, MC, NL, PT, RO, SE, SI, SK, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:

— *with international search report*

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.